ABSTRACT

A system and method for designing ICs, including the steps of: analyzing and optimizing a target IC design based on design-specific objectives; partitioning the optimized target IC design into pre-defined standard-cells from one or more libraries and creating design-specific cells specifically having unique functionality and characteristics not found amongst the standard-cells; identifying and determining a minimal subset of the standard-cells and design-specific cells, the interconnection of which represents the target IC design; generating the necessary views, including layout and characterizing of the design-specific cells included in a unique, minimal subset, wherein the IC design is subject to objectives and constraints of the target IC.